REMARKS

Claims 1, 4-7, 10-13, 15, 18, 21-23, and 25-27 are pending. Claims 1, 7, 15, and 18 are in independent form.

Applicant thanks the Examiner for the courtesy of a telephone discussion on June 8, 2007 at which time Applicant's representative apologized for the failure to include the Declaration under 37 C.F.R. § 1.131 discussed in the response filed May 3, 2007.

Submitted herewith is a copy of the Declaration, as discussed.

Applicant asks that all claims be allowed. Please apply the three-month extension of time fee and any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: June 8, 2007

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Attorney's Docket No.: 10559-602001 / P12886

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : William R. Wheeler, et al. Art Unit: 2123
Serial No.: 09/994,574 Examiner: Russell L. Guill
Filed : November 26, 2001
Title : UNIFIED DESIGN PARAMETER DEPENDENCY MANAGEMENT METHOD AND APPARATUS

Mail Stop AMENDMENT
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. § 1.131

We, William R. Wheeler, Timothy J. Fennell, and Matthew J. Adiletta hereby declare:

1. That we are the inventors of the claims in the patent application identified above.

2. That in an Office Action dated January 5, 2007, claims were rejected as being unpatentable under 35 U.S.C. § 103(a) as being obvious over U.S. Patent Publication No. 2002/0023250 to Yumoto et al. (hereinafter "Yumoto"), in combination with one or more other references.

3. That prior to June 8, 2001, and thus necessarily before the filing date of Yumoto, we had worked in this country to complete the conception and reduction to practice of the invention recited in present pending claims 1, 4-7, 10-13, 15, 18, 21-23, and 25-27 of the application identified above.

4. That, in support, the attached EXHIBITS A, B, C, D, E are submitted herewith.

5. That EXHIBIT A shows a history of source file checkins made during the development of a software application prior to June 8, 2001, including a checkin identified as "version.h".

6. That EXHIBIT B shows the chronological history of the changes made to "version.h" and the applications of labels to "version.h," including application of the label "0.141" prior to June 8, 2001.

7. That "version.h" labeled "0.141" is thereby shown to have actually existed prior to June 8, 2001.

8. That EXHIBITS C, D, E show actual results obtained using the software application built using all source files labeled "0.141," including "version.h."

9. That EXHIBITS C, D, E all show, on the left, a view of central database and, on the right, one or potentially many graphical views of part of an electrical circuit that are automatically updated based on changes to the values in the central database using identifiers of the signal properties in the central database, namely, Verilog tic defines.

10. That the labeling of the AND gate in red in EXHIBIT C indicates a design discrepancy resulting from the anding of Input1 and Input2, where bit spec MSB1:0 indicates a signal with a width of 31 bits and bit spec MSB2:0 indicates a signal with a width of 32 bits.

11. That the software application built from source files labeled "0.141," including "version.h," is thereby shown to have

indicated design discrepancies in signal properties the illustrated part of the electrical circuit prior to June 8, 2001.

12. That EXHIBIT D shows a user interface for the modification of the value associated with MSB1 from 30 to 31 in the central database.

13. That the software application built from source files labeled "0.141," including "version.h," is thereby shown to access and modify the values of identifiers of signal properties in the central database.

14. That, in EXHIBIT E, as soon as the "OK" button in Exhibit D is clicked, the red AND gate turns grey and is labeled "32", indicating that the design discrepancy has been eliminated.

15. That the software application built from source files labeled "0.141," including "version.h," is thus shown to automatically update the logic design to reflect modification of the values of identifiers of signal properties in the central database.

16. That the dates on EXHIBIT A and EXHIBIT B, all of which are prior to June 8, 2001, have been blocked out.

17. That we hereby declare that all statements made herein of our knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false

statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Dated: 4/17/07

William R. Wheeler

Dated: 4/18/2007

Timothy J. Fennell

Dated: 4-23-2007

Matthew J. Adiletta